WHAT IS CLAIMED IS:

1. An apparatus comprising:

a plurality of processor groups each having a plurality of processor switch chips each having a plurality of processors and a processor crossbar, each processor connected to the processor crossbar;

a plurality of switch groups each having a plurality of switch crossbar chips each having a plurality of switch crossbars each connected to a processor crossbar in each processor group, wherein no two switch crossbars in a switch group are connected to the same processor crossbar;

a plurality of memory groups each having a plurality of memory switch chips each having a plurality of memory controllers and a memory crossbar, each memory controller connected to the memory crossbar, each memory crossbar in each memory group connected to all of the switch crossbars in a corresponding one of the switch groups, wherein no two memory groups are connected to the same switch group; and

a plurality of memory chips each having a plurality of memory tracks each having a plurality of shared memory banks, each memory track connected to a different one of the memory controllers.

2. A method comprising:

implementing a plurality of processor groups each having a plurality of processor switch chips each having a plurality of processors and a processor crossbar, each processor connected to the processor crossbar;

implementing a plurality of switch groups each having a plurality of switch crossbar chips each having a plurality of switch crossbars;

connecting each switch crossbar to a processor crossbar in each processor group, wherein no two switch crossbars in a switch group are connected to the same processor crossbar;

implementing a plurality of memory groups each having a plurality of memory switch chips each having a plurality of memory controllers and a memory crossbar, each memory controller connected to the memory crossbar;

connecting each memory crossbar in each memory group to all of the switch crossbars in a corresponding one of the switch groups, wherein no two memory groups are connected to the same switch group;

implementing a plurality of memory chips each having a plurality of memory tracks each having a plurality of shared memory banks; and

connecting each memory track to a different one of the memory controllers.

3. An apparatus for use in a scalable graphics system comprising:

a processor switch chip having a plurality of processors each connected to a processor crossbar; and

a memory switch chip having a plurality of memory controllers each connected to a memory crossbar and controlling a shared memory bank; and wherein

the memory crossbar is connected to the processor crossbar.

4. The apparatus of claim 3, further comprising an intermediate switch chip having a switch crossbar, the switch crossbar connected between the processor crossbar and the memory crossbar.

5. The apparatus of claim 3, wherein each memory controller is connected to a memory chip having a shared memory bank.

6. The apparatus of claim 3, wherein the memory switch chip comprises a memory bank connected to the memory controller.

7. The apparatus of claim 3, wherein the apparatus is used for the purposes of ray-tracing.

8. A method comprising:

implementing a processor switch chip having a plurality of processors each connected to a processor crossbar;

implementing a memory switch chip having a plurality of memory controllers each connected to a memory crossbar and controlling a shared memory bank; and

connecting the memory crossbar to the processor crossbar.

9. The method of claim 8, further comprising:

implementing an intermediate switch chip having a switch crossbar; and

connecting the switch crossbar between the processor crossbar and the memory crossbar.

10. The method of claim 8, further comprising:

implementing a memory chip having a shared memory bank; and

connecting each memory chip to one of the memory controllers.

11. The method of claim 8, wherein the memory switch chip comprises a memory bank connected to the memory controller.